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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,337	04/12/2001	Van Hoa Lee	AUS920010196US1	3774

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,337	LEE ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Drawings dated 08/07/01.

2. Claims 1-16 are presented for examination.

Claim Objections

3. Claim 4, 9 and 14 are objected to because of the following informalities: "the nodal time base source " beginning on line 6 of claims 4 and 9 and on line 7 of claim 14 should be changed to "a nodal time base source" because it is the first recitation of a nodal time base source.

Also, in claim 9, the typographical error "salve" should be changed to "slave" on line 4 of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 5, 6, 8, 10, 11, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Dove et al., U.S. Patent 5,938,765 (hereinafter "Dove").

6. As to claim 6, Dove teaches (as per claim 6) a system for booting a non-uniform-memory-access (NUMA) machine comprising:

a. configuring (initializing) a plurality of standalone, symmetrical multiprocessor systems (each node is a symmetrical multiprocessor) to operate within a NUMA system (each of the nodes are configured prior to be used in a NUMA system) [col. 5 lines 58-62];

b. assigning a NUMA identification (node_id field) to each of the multiprocessing systems, wherein each identification is unique [col. 7 line 58 through col. 8 line 11];

c. booting the multiprocessor systems in NUMA mode in one-pass, wherein memory coherency (address regions have unique address and are therefore coherent) is established at the beginning of the execution of the system firmware [col. 6 lines 33-36].

7. As to claim 8, Dove taught the system according to claim 6 as described above. Dove taught the method according to claim 6 further comprising:

a. a plurality of nodal selection mechanisms which select a nodal master (BSP is interpreted to be the master because it controls the nodal system during its boot, the BSP must be selected from among the plurality of processors) within each multiprocessing system and designate all other processors within each system as nodal slave processors (other processors are interpreted to be slaves) [col. 7 line 58-60];

b. a NUMA selection mechanism (either by a user or by software) which selects a NUMA master processor (operating system loader or master processor) from among the separate nodal master processors and designates all other nodal master processors as NUMA slave processors (because one processor is selected as a master it is interpreted that all other processors are considered as slaves) [col. 9 line 61 through col. 10 line 7].

8. As to claim 10, Dove taught the system according to claim 8 as described above. Dove further taught wherein the NUMA processor:

a. loads a single operating system into NUMA system memory (bringing all nodes into a multimode environment and loads the operating system) [col. 10 lines 2-28];

b. transfers control to the operating system (loads the operating system) [col. 10 lines 2-28]; and

c. runs operating system code which assigns all slave processor to a designated place within the NUMA operating system (the operating system gains access to the MP table which identifies the processors on the system which would be used to allow any processor access to memory in any other node for processing) [col. 10 lines 25-28].

9. As to claims 1, 3, 5, 11 and 15, Dove taught the claimed system therefore he also taught the claimed method and computer program product.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2, 7, 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove in view of Northcutt et al. U.S. Patent 6,678,741 (hereinafter "Northcutt").

12. As to claim 7, Dove taught the system according to claim 6 as described above. Dove further taught

a. a host testing component which configures and tests (diagnostics are run) host processors and memory [col. 2 lines 10-19];

b. a NUMA testing component which configures (remapping memory) [col. 6 lines 6-11] and tests NUMA memory (the initialization of the multimode system uses the standard BIOS for single-node system, which would runs diagnostics on memory) [col. 6 lines 48-56];

c. an adapter-configuring component (system interconnect interface) which configures NUMA adapters to connect each multiprocessing system to the NUMA system and initializing all the host processors (by re-programming the addresses based on the MP Tables and the node configuration table) [figure 2, col. 3 lines 12-19]; and

d. a releasing mechanism (a "hard" or "soft" reset) which releases all host processors to execute system firmware [col. 6 lines 51-56].

Dove does not expressly disclose a software loading mechanism which loads a firmware image into local memory and informs a hardware system console of the firmware version.

Dove also does not expressly, disclose a receiving component which receives a confirmation from the hardware system console that the firmware version is the same for all multiprocessing systems in the NUMA system.

Specifically, Dove is silent with respect to the firmware and the version thereof used in his system. However, it is inherent that each multiprocessing system must use firmware for at least communication purposes. This firmware must be loaded into the local of each multiprocessing system for at least communication purposes to take place.

Northcutt teaches a system having a software loading mechanism which loads a firmware image (upon booting or powering up) into local memory (of the first device and second device) and informs a hardware system consoles (mechanism to determine the firmware version) of the firmware version (sending a set of an initial protocol parameters) [col. 4 line 63 through col. 5 line 49].

Northcutt further teaches receiving component which receives a confirmation (compares and determines the if firmware is synchronized) from the hardware system console that the firmware version is the same for all multiprocessing systems (first and second devices or server) [col. 5 lines 31-49].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dove to inform a hardware system console of the version and confirm the version is the same for all the multiprocessing systems as taught by Northcutt in the multiprocessing system in the NUMA system of Dove. One of ordinary skill in the art would have made the modification because Northcutt teaches that doing so would desirable reduce the inoperability due to incompatible firmware in the systems for communication [col. 1 line 63 et seq.]. Further, Northcutt teaches that the firmware would be desirable updated.

13. As to claims 2 and 12, Dove as modified taught the claimed system therefore he also taught the claimed method and computer program product.

14. As to claim 16, Dove substantially taught a system for booting a non-uniform-memory-access (NUMA) machine comprising:

a. a plurality of hardware-configuring component which configure (initialize) a plurality of standalone, symmetrical multiprocessor systems (each node is a symmetrical

multiprocessor) to operate within a NUMA system (each of the nodes are configured prior to be used in a NUMA system) [col. 5 lines 58-62];

b. an identification component which assigns a NUMA identification (node_id field) to each of the multiprocessing systems, wherein each identification is unique [col. 7 line 58 through col. 8 line 11];

c. a booting mechanism which boots the multiprocessor systems in NUMA mode in one-pass, wherein memory coherency (address regions have unique address and are therefore coherent) is established at the beginning of the execution of the system firmware [col. 6 lines 33-36].

d. a plurality of nodal selection mechanisms which select a nodal master (BSP is interpreted to be the master because it controls the nodal system during its boot, the BSP must be selected from among the plurality of processors) within each multiprocessing system and designate all other processors within each system as nodal slave processors (other processors are interpreted to be slaves) [col. 7 line 58-60];

e. a NUMA selection mechanism (either by a user or by software) which selects a NUMA master processor (operating system loader or master processor) from among the separate nodal master processors and designates all other nodal master processors as NUMA slave processors (because one processor is selected as a master it is interpreted that all other processors are considered as slaves) [col. 9 line 61 through col. 10 line 7].

f. a host testing component which configures and tests (diagnostics are run) host processors and memory [col. 2 lines 10-19];

g. a NUMA testing component which configures (remapping memory) [col. 6 lines 6-11] and tests NUMA memory (the initialization of the multimode system uses the standard BIOS for single-node system, which would runs diagnostics on memory) [col. 6 lines 48-56];

h. an adapter-configuring component (system interconnect interface) which configures NUMA adapters to connect each multiprocessing system to the NUMA system and initializing all the host processors (by re-programming the addresses based on the MP Tables and the node configuration table) [figure 2, col. 3 lines 12-19]; and

i. a releasing mechanism (a "hard" or "soft" reset) which releases all host processors to execute system firmware [col. 6 lines 51-56].

j. a switching mechanism which switches the nodal slave processors in each multiprocessing system to a hyper-visor environment in which the nodal slave processors become NUMA slave processors (once loaded the operating system is able to access resources from any multiprocessor system as needed) [col. 10 lines 2-28].

Dove does not expressly disclose a software loading mechanism which loads a firmware image into local memory and informs a hardware system console of the firmware version.

Dove also does not expressly, disclose a receiving component which receives a confirmation from the hardware system console that the firmware version is the same for all multiprocessing systems in the NUMA system.

Specifically, Dove is silent with respect to the firmware and the version thereof used in his system. However, it is inherent that each multiprocessing system must use firmware for at

least communication purposes. This firmware must be loaded into the local of each multiprocessing system for at least communication purposes to take place.

Northcutt teaches a system having a software loading mechanism which loads a firmware image (upon booting or powering up) into local memory (of the first device and second device) and informs a hardware system consoles (mechanism to determine the firmware version) of the firmware version (sending a set of an initial protocol parameters) [col. 4 line 63 through col. 5 line 49].

Northcutt further teaches receiving component which receives a confirmation (compares and determines the if firmware is synchronized) from the hardware system console that the firmware version is the same for all multiprocessing systems (first and second devices or server) [col. 5 lines 31-49].

15. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dove to inform a hardware system console of the version and confirm the version is the same for all the multiprocessing systems as taught by Northcutt in the multiprocessing system in the NUMA system of Dove. One of ordinary skill in the art would have made the modification because Northcutt teaches that doing so would desirable reduce the inoperability due to incompatible firmware in the systems for communication [col. 1 line 63 et seq.]. Further, Northcutt teaches that the firmware would be desirable updated.

16. Claims 4, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove in view of Arndt et al., U.S. Patent 5,802,378 (hereinafter "Arndt").

17. As to claim 9, Dove taught the system according to claim 8 as described above. Dove further taught the system comprising:

a. a switching mechanism which switches the nodal slave processors in each multiprocessing system to a hyper-visor environment in which the nodal slave processors become NUMA slave processors (once loaded the operating system is able to access resources from any multiprocessor system as needed) [col. 10 lines 2-28].

Dove does not expressly disclose a handshaking mechanism which performs one-to-one handshaking between the nodal master processor and each nodal slave processor within a multiprocessor system, wherein the handshaking synchronizes the time base register of all nodal slaves with the nodal time base source.

Arndt teaches a multiprocessor system that performs one-to-one handshaking between a nodal master (one of the processors of 3A through 3N) and each nodal slave processor (other processors are interpreted to be slaves) within a multiprocessor system, wherein the handshaking synchronizes (performs clock synchronization) the time base register (time base facility 12) of all nodal slave processors with the nodal time base source (system clock 52) [col. 5 lines 26-34, col. 5 lines 50-65, and figures 1-4].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dove by synchronizing the time bases of the nodal master and slaves as taught by Arndt. Dove and Arndt are both directed toward multiprocessor systems. One of ordinary skill would have made the modification because the modification of Dove using the teachings of

Arndt would reduce if not eliminate synchronization and timing problems [Arndt – col. 2 lines 34-49] within a multiprocessor system such as that of Dove.

18. As to claims 4 and 14, Dove together with Arndt taught the claimed system therefore together they also teach the claimed method and computer program product.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,611,911 to O'Shea et al. This patent teaches selecting a bootstrap processor within a multiprocessor system.

U.S. Pat. No. 6,351,795 to Hagersten. This patent teaches coherent memory in a NUMA system.

U.S. Pat. No. 5,970,439 to Levine et al. This patent teaches using a time base register to synchronize multiple processors.

U.S. Pat. No. 6,584,560 to Kroun et al. This patent teaches a method for booting a multiprocessor system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
May 10, 2004

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